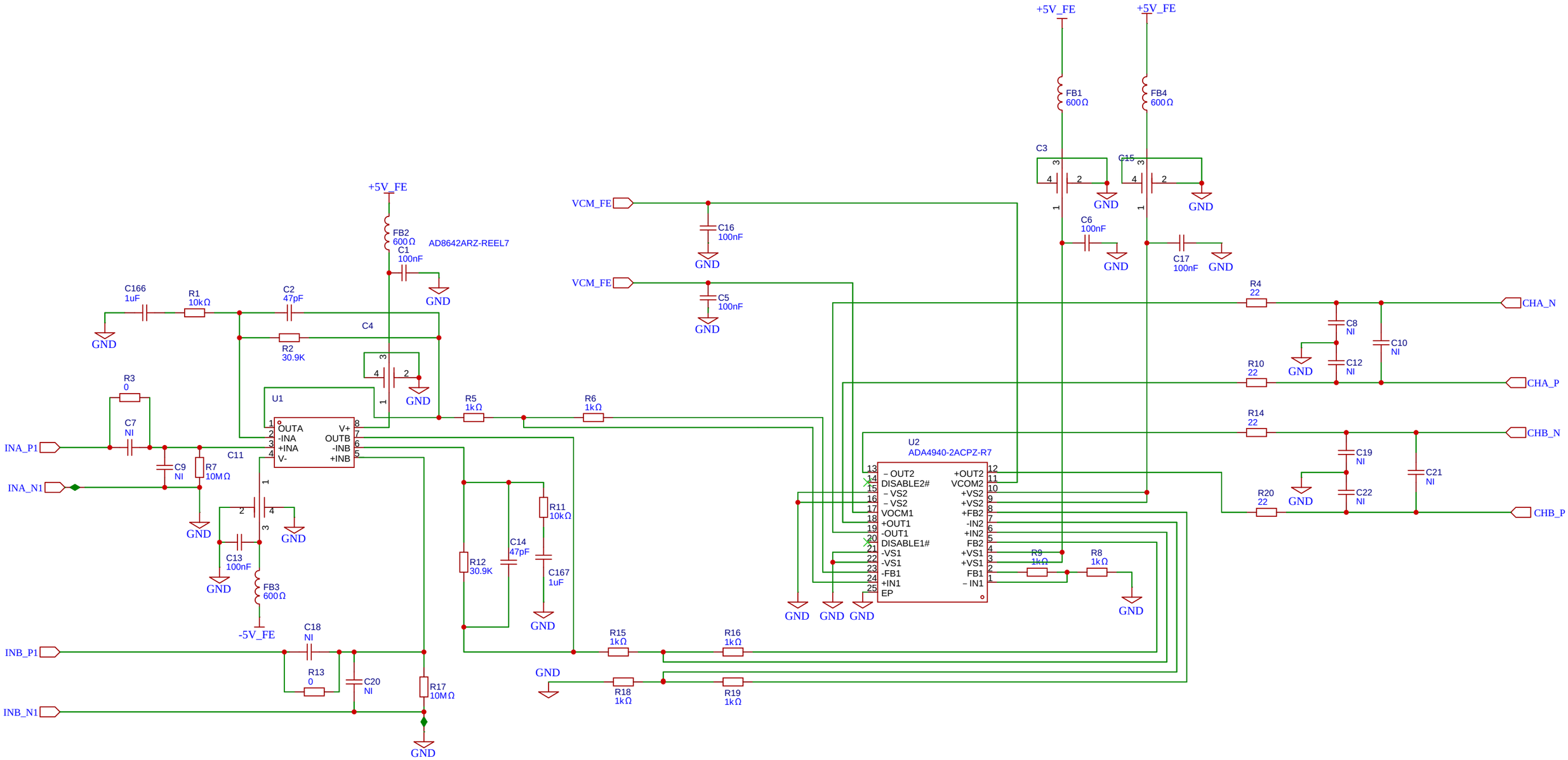
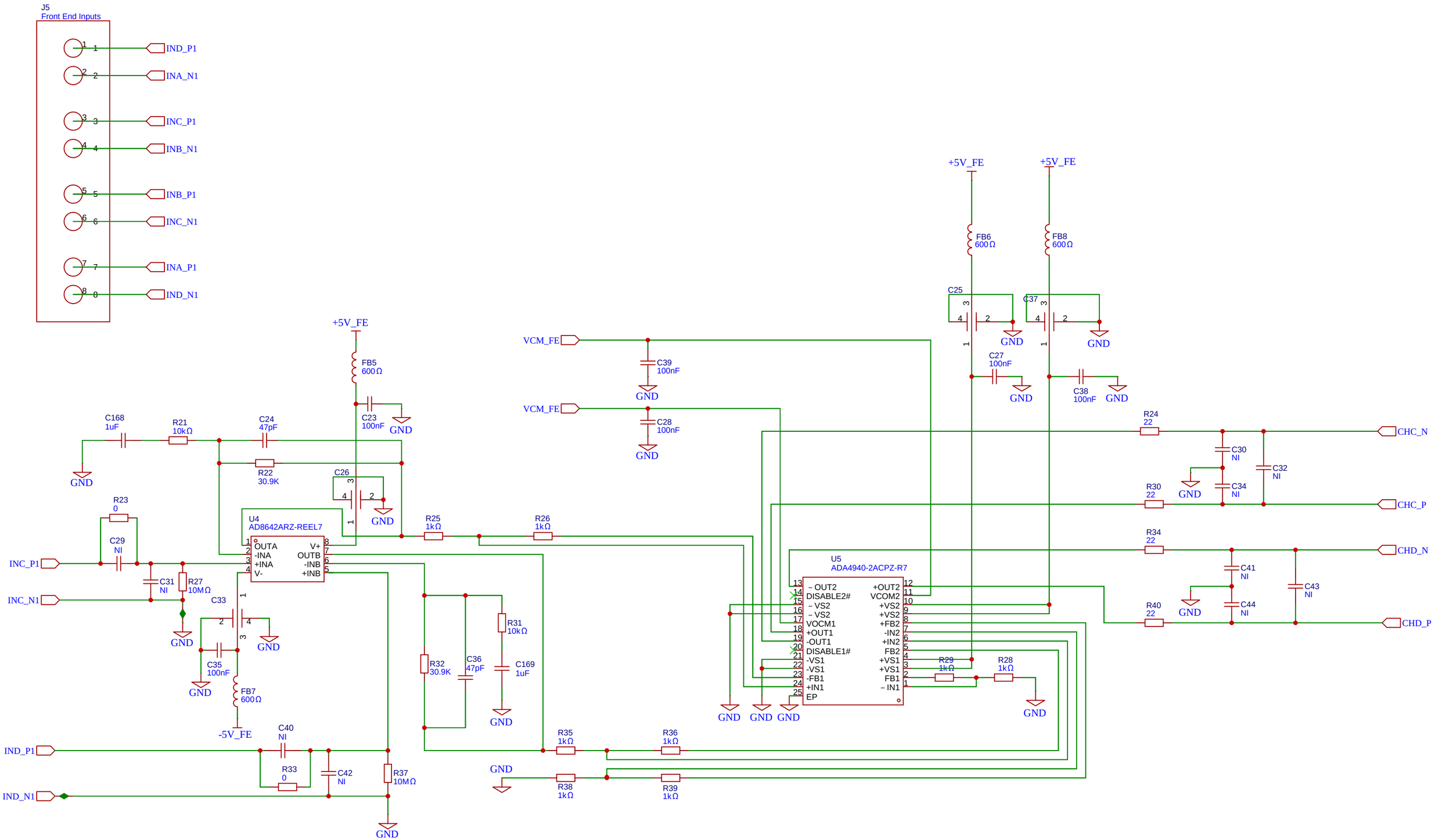


Front End Channels (A & B)

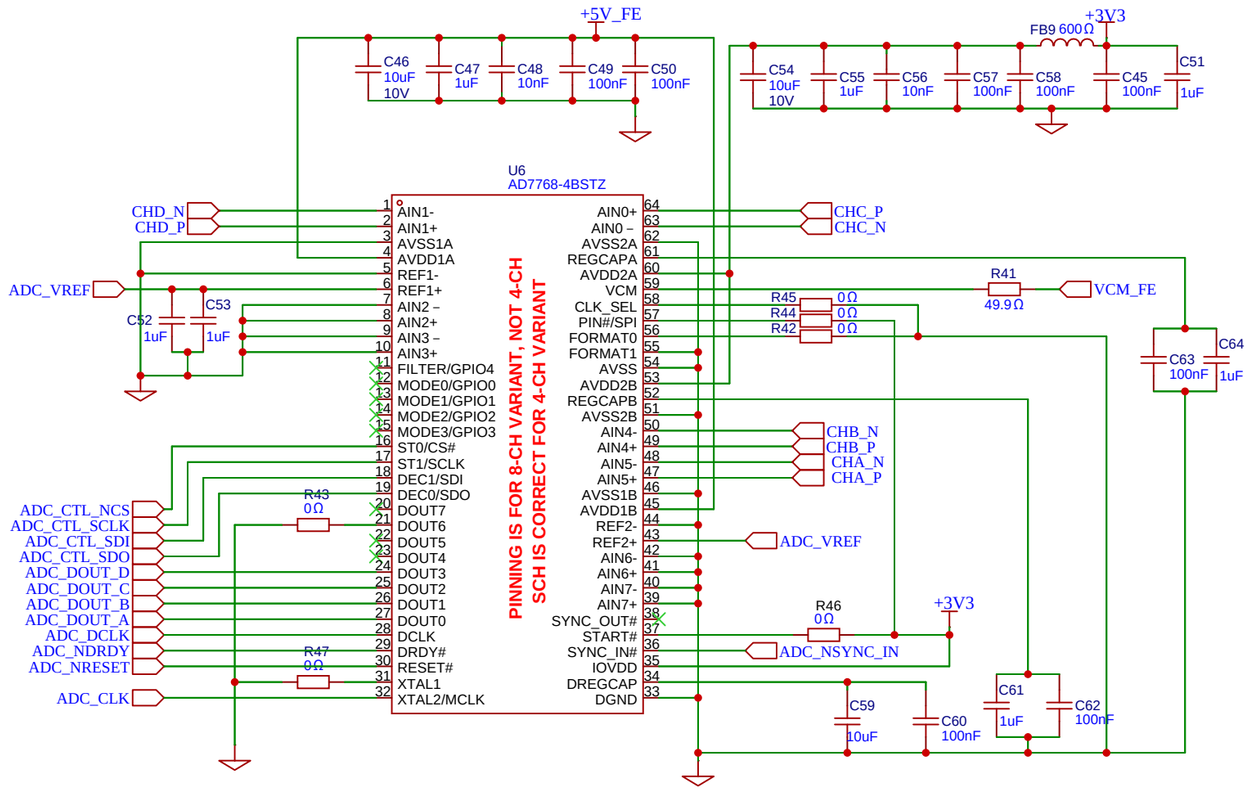
TITLE: TagV2p2_r4		REV: 3
嘉立创EDA	Company: Project CETI	Sheet: 1/9
	Date: 2023-05-12	Drawn By: Shreya Singh



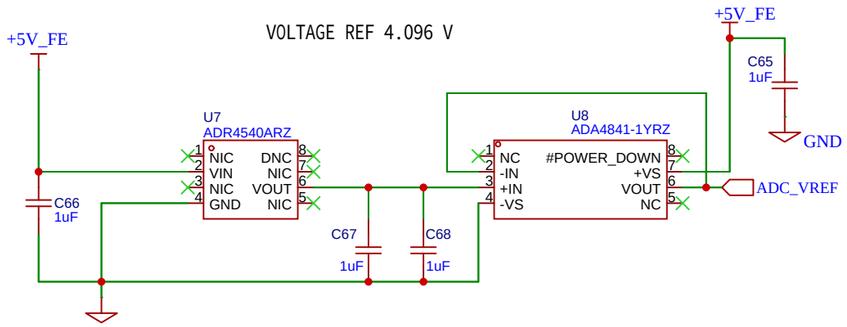
Front End Channels (C & D)

TITLE: TagV2p2_r4		REV: 3
嘉立创EDA	Company: Project CETI	Sheet: 2/9
	Date: 2023-05-12 Drawn By: Shreya Singh	

24-BIT ADC

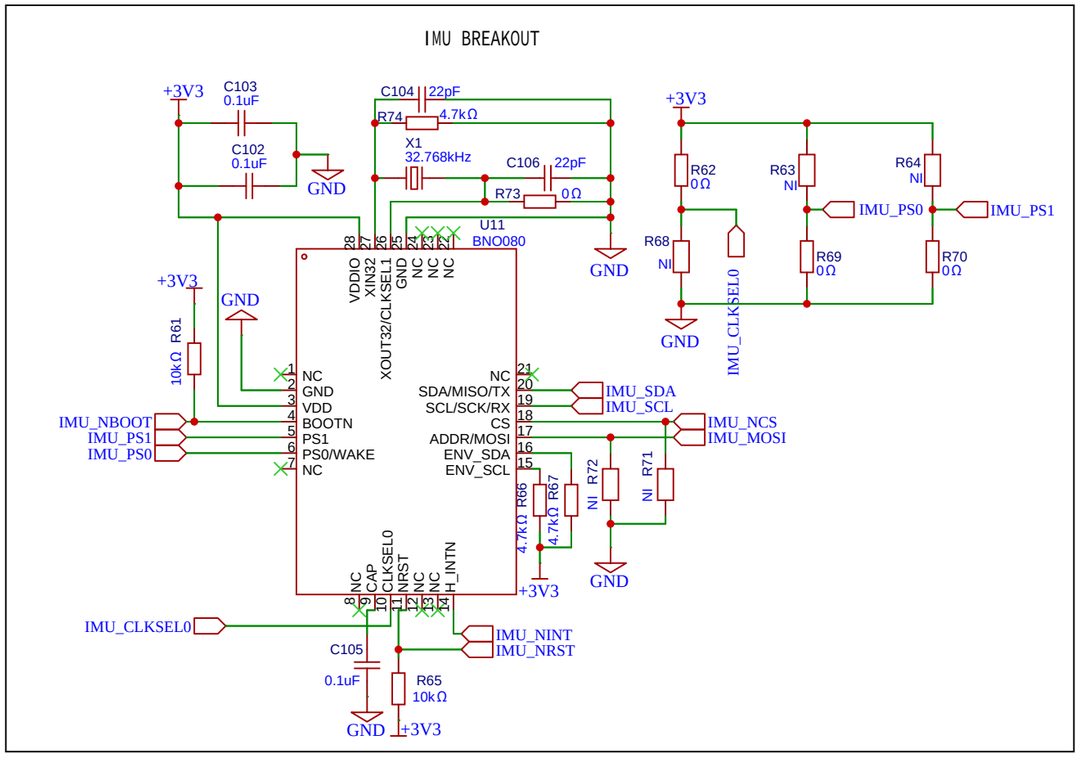


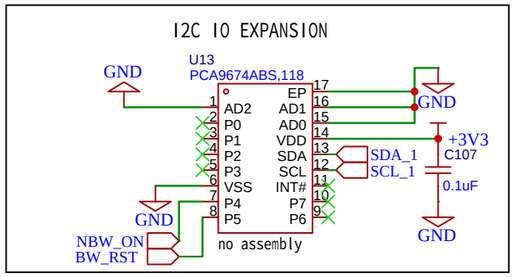
VOLTAGE REF 4.096 V

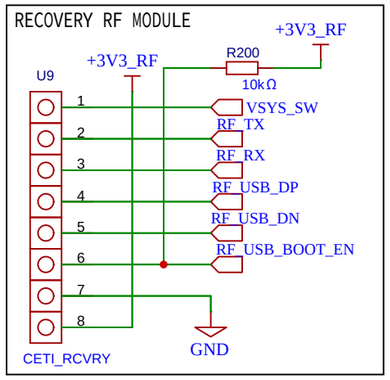


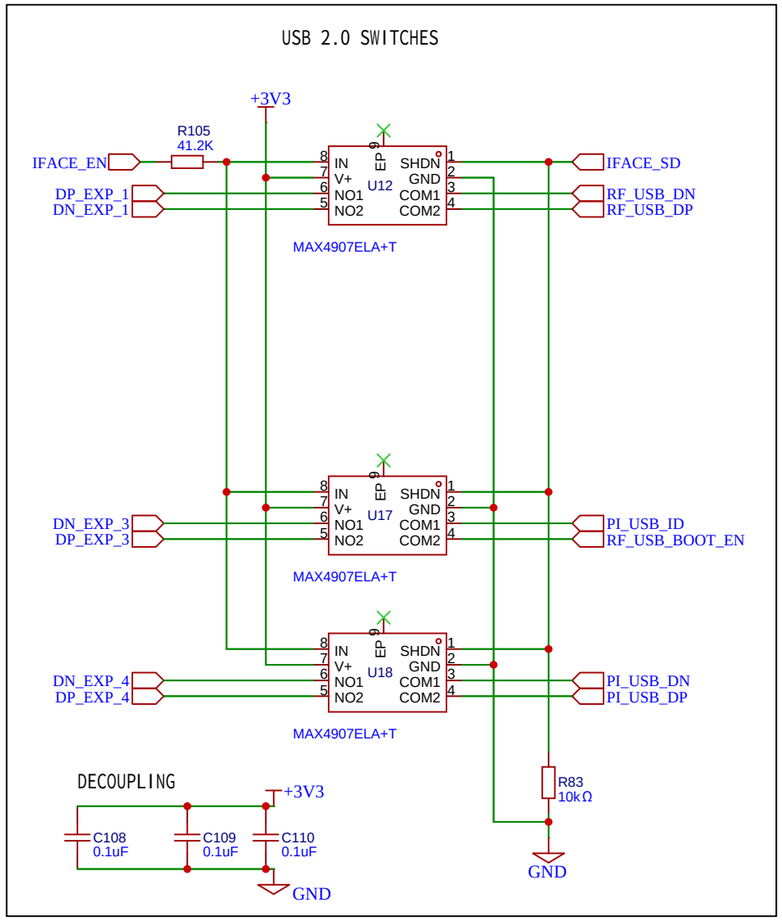
24-BIT 4-CHANNEL ADC

TITLE: TagV2p2_r4		REV: 4
嘉立创EDA	Company: Project CETI	Sheet: 3/9
	Date: 2023-05-12	Drawn By: Shreya Singh

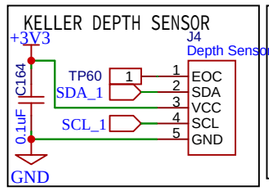


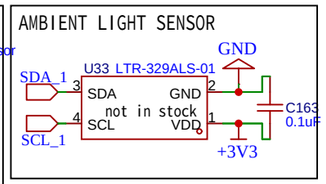


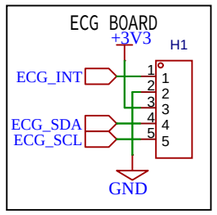


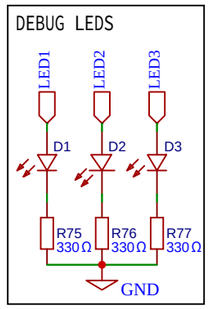


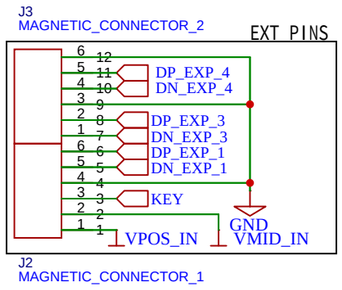
I2C PERIPHERALS

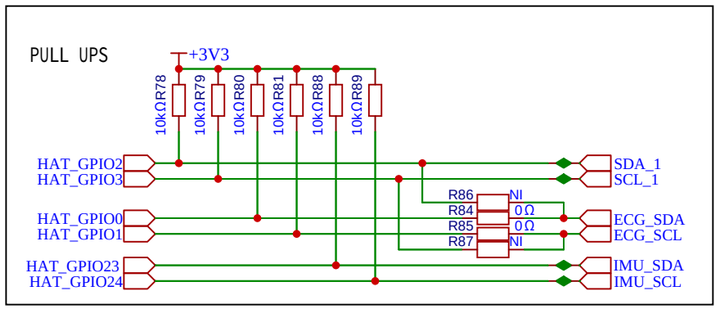


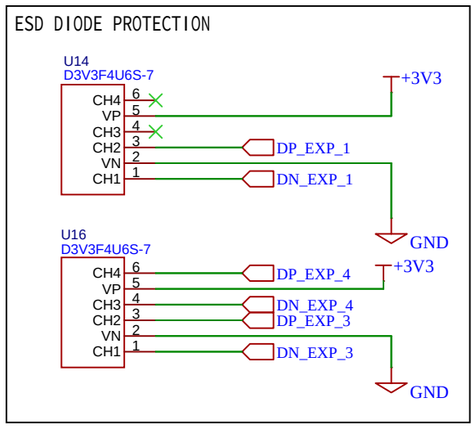








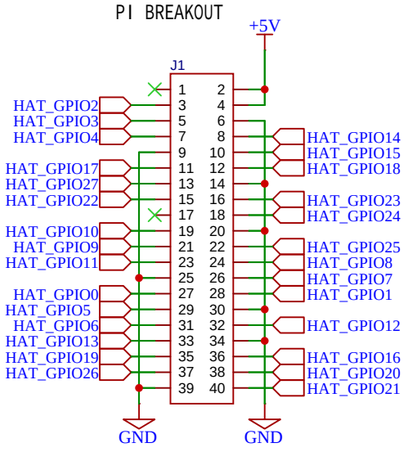




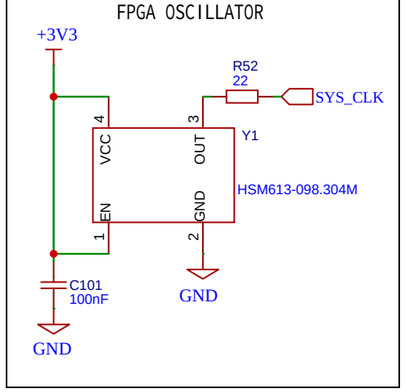
Sensors & Peripherals

TITLE: TagV2p2_r4	REV: 3
Company: Project CETI	Sheet: 4/9
Date: 2023-05-12	Drawn By: Shreya Singh

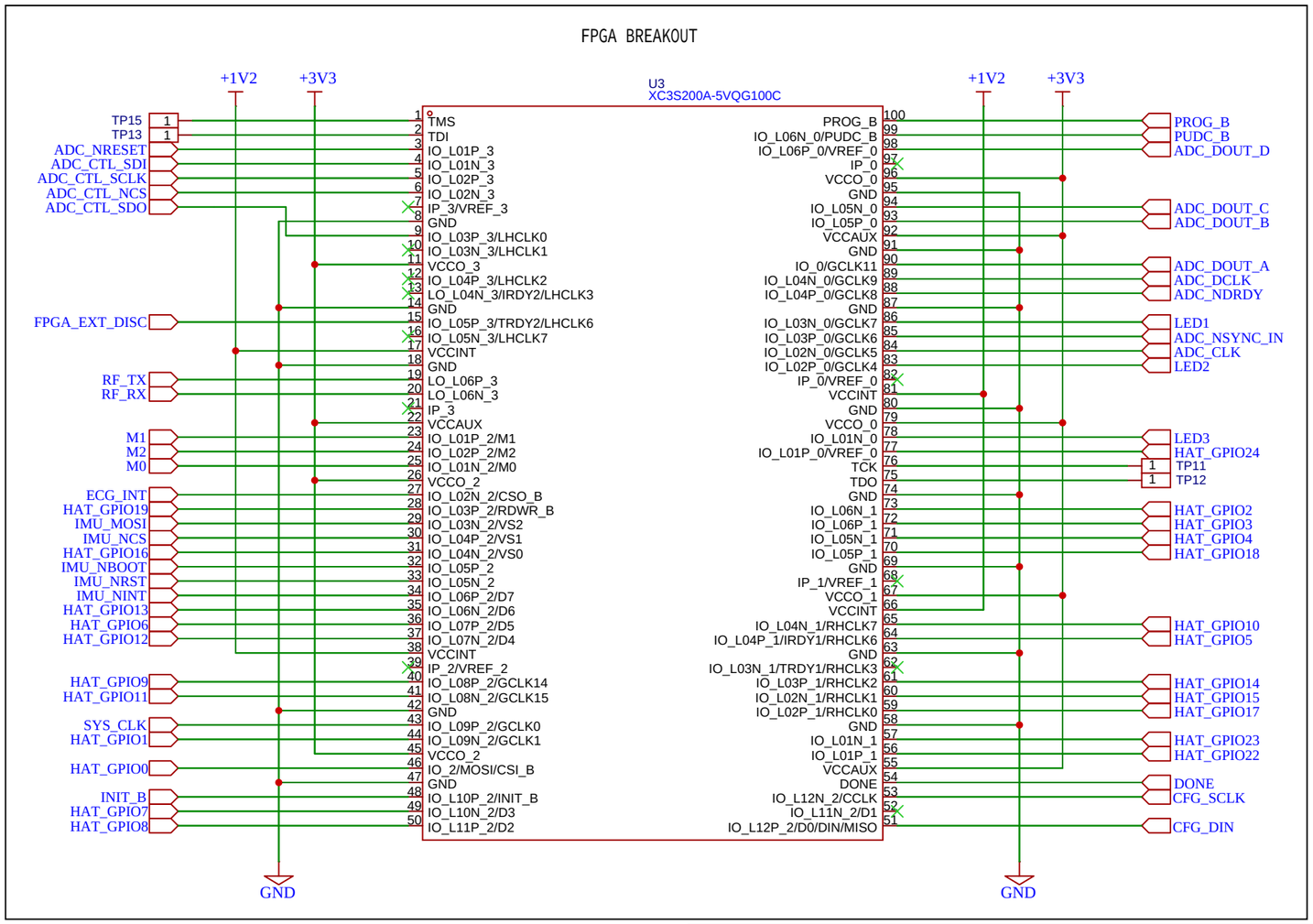
PI BREAKOUT



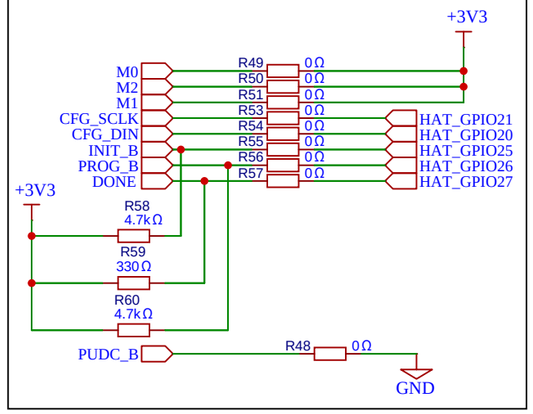
FPGA OSCILLATOR



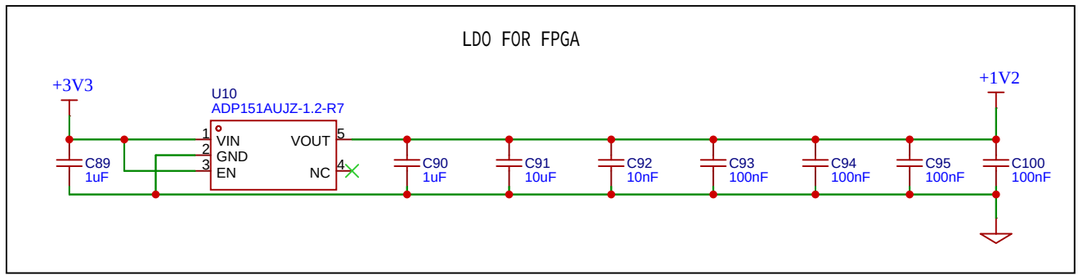
FPGA BREAKOUT



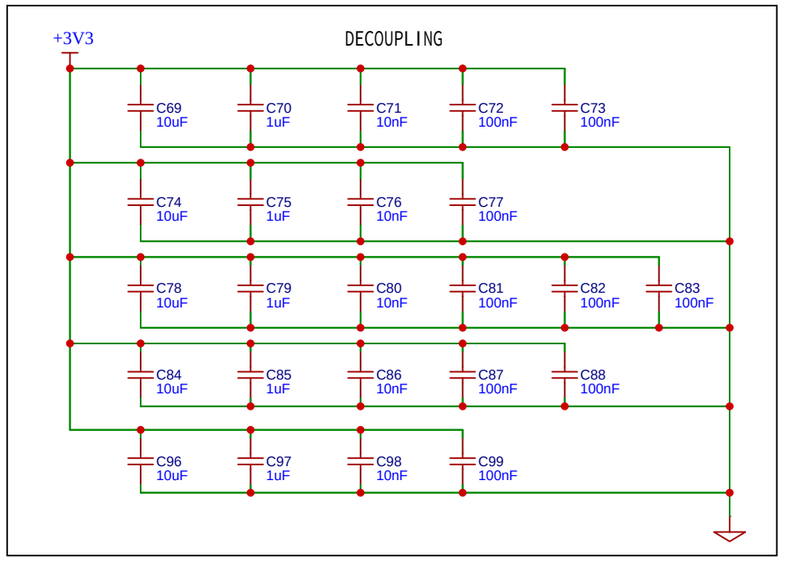
JUMPERS



LDO FOR FPGA

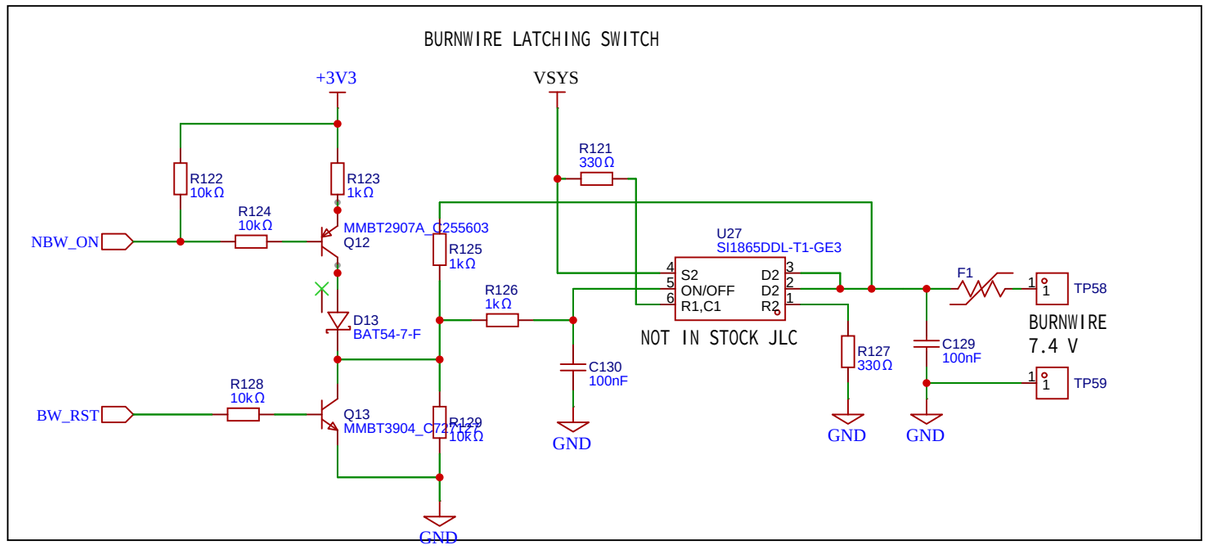


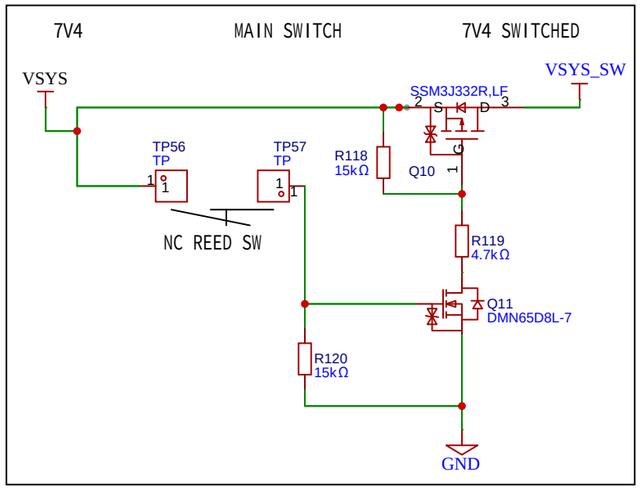
DECOUPLING

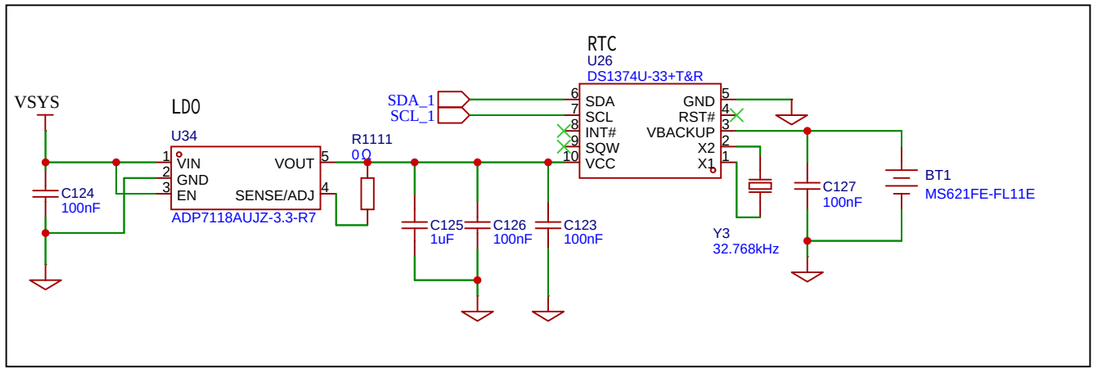


MCU & FPGA

TITLE: TagV2p2_r4		REV: 3
嘉立创EDA	Company: Project CETI	Sheet: 5/9
	Date: 2023-05-12 Drawn By: Shreya Singh	

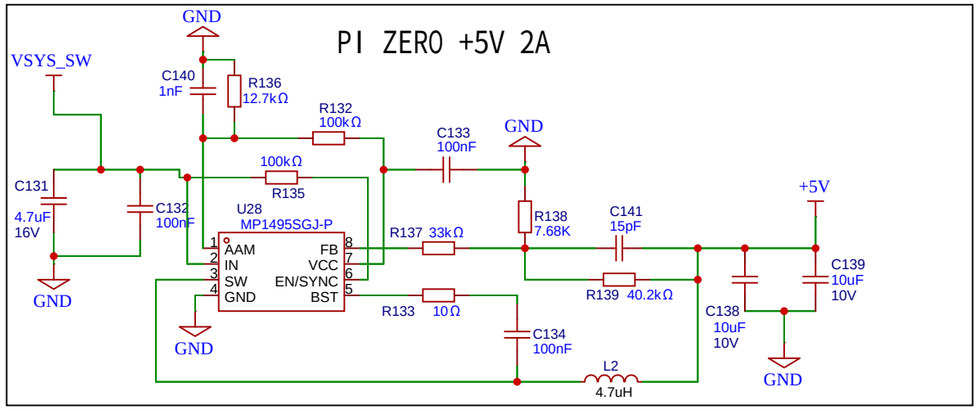


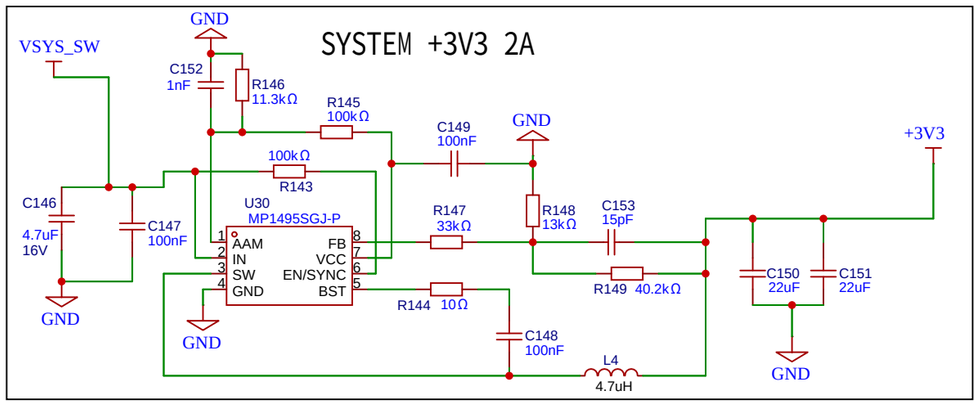


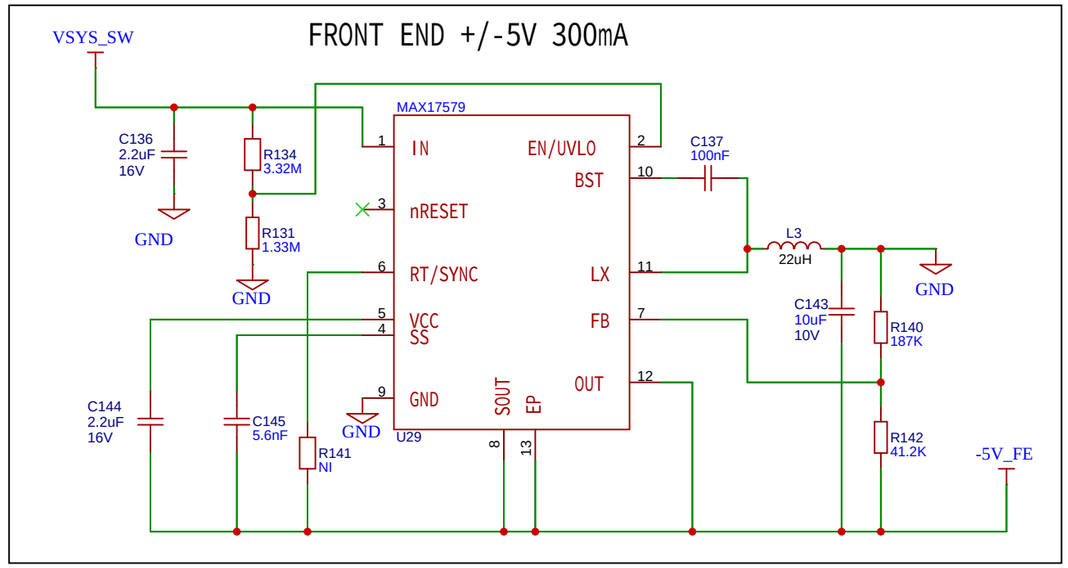


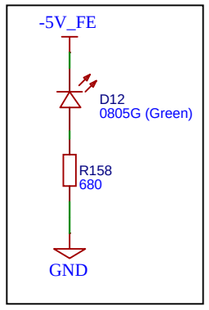
Burnwire Drive & Reed Switches

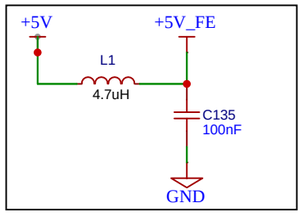
TITLE: TagV2p2_r4	REV: 4
Company: Project CETI	Sheet: 6/9
Date: 2023-05-12 Drawn By: Shreya Singh	











Power

TITLE: TagV2p2_r4		REV: 3
嘉立创EDA	Company: Project CETI	Sheet: 7/9
	Date: 2023-05-12 Drawn By: Shreya Singh	

PROTECTION AND FUEL GAUGE

EXTERNAL CHARGER CONNECTIONS

VPOS_IN
D5 BZX584C10V
Q3 SSM3J332R,LF
Q4 SSM3J332R,LF
R90 15kΩ
VSYS
1kΩ R92
IFACE_EN
Q5 DMN65D8LW-7
OK component?

EXTERNAL INTERFACE - ISOLATION SWITCHES

VMID_IN
D6 BZT52C5V6S
Q6 SSM3J332R,LF
Q7 SSM3J332R,LF
R102 15kΩ
1kΩ R103
IFACE_EN
Q8 DMN65D8LW-7
BAT_MID_FUSED
F2 0ZCH0050FF2G
BAT_MID
R101 CRM2010-JW-4R7ELF

SDA_1
SCL_1
R98 150Ω
R99 150Ω

C112 1000pF
C113 1000pF
Q1 IRLML0030TRPBF
Q2 IRLML0030TRPBF
U21 MINISMDC200F/16-2
BAT_POS
R97 1kΩ
R93 1kΩ
R91 470Ω
R94 1kΩ
R95 150Ω
R96 1kΩ
C114 470nF
BAT_MID_FUSED
R100 1kΩ
C116 0.1uF
C115 0.1uF
D7 BZT52C5V6S
D8 BZT52C5V6S
D9 BAT54S_C408389
U19 DS2778G
NO ASSEMBLY
PLS
SDA/DQ
SCL/OVD
PIO
VB
CSO
SRC
SNS
VDD
VIN2
VIN1
CP
EPAD
VSS
R104 0.025R 1W
BAT_NEG

EXTERNAL INTERFACE ENABLE

VSYS
VPOS_IN
D11
D14
U24 ADP7118AUJZ-3.3-R7
VIN
GND
EN
VOUT
SENSE/ADJ
C117 0.1uF
R501 0
C119 1uF
+3V3_EXT
C120 0.1uF
WINDOW COMPARATOR
R107 15kΩ
WIN_HI
R111 3.3kΩ
WIN_LO
R116 15kΩ
U35 LMV393IDR
1OUT
1IN-
1IN+
GND
VCC+
2OUT
2IN-
2IN+
WIN_HI
WIN_LO
R108 15kΩ
E13
IFACE_EN
R114 1kΩ
KEY
R109 100Ω
KEY_IN
R110 4.7kΩ
D10 BAT54S_C408389
+3V3_EXT
ESD
Q9 DMN65D8LW-7
FPGA_EXT_DISC
R82 1kΩ

KEY_IN VOLTAGE MUST BE BETWEEN 1.5V AND 1.8V TO ENABLE I/O VIA EXT PIN INTERFACE

TEMPERATURE MONITORING

+3V3
C162 0.1uF
GND
U25 ADT7461ARZ-REEL
VDD
D+
D-
THERM#
SCLK
SDATA
ALERT#/THERM2#
GND
SCL_1
SDA_1
TSENS_A
TSENS_K
GND

TO TEMP SNS DIODE BONDED TO BATTERY CELLS

BMS

TITLE: TagV2p2_r4		REV: 3
嘉立创EDA	Company: Project CETI	Sheet: 8/9
	Date: 2023-05-12 Drawn By: Shreya Singh	

CHANGE LOG

REV 4 10/19/23 CUMMINGS:

* CONNECTED GPIO13 TO RF 3V3 SO SW CAN TURN IT OFF AND ON.
* ADD PULL UP ON RECOVERY BOOT_EN LINE
* DEPTH SENSOR POSITION ADJUSTED IN LAYOUT (MICHAEL)
* UPDATED FRONT END TO ADD HPF POLE
* E13 SHOULD NOT BE INCLUDED IN BOM. REMOVED (MATT 10/23/23)

MUST HAVE

MORE EXPLANATORY NOTES

NICE TO HAVE

DRAW OP AMPS AND COMPARATORS AS FUNCTIONAL SYMBOLS NOT BOX SYMBOLS
ADC SYMBOL IS DRAWN AS THE 8-CH INCORRECT PIN LABELS FOR 4-CH
CETI/SEAS LOGO ON TEMPLATE
FIX BMS IC SO PIN NAMES ARE LEGIBLE

NOTES, ISSUES AND TODO LIST

Schematic	TagV2.2_Rev4	Update Date	2023-10-23
		Create Date	2023-10-16
Page	Notes and Todo	Part Number	JLCPCB-002
Drawed	EasyEDA Pro	TagV2p2_r4	
Reviewed	EasyEDA Pro		
		VER 3 / SIZE A4 / PAGE 9 OF 9	
EasyEDA		EasyEDA.com	